A 180 nm CMOS Low Noise Amplifier with Increased linearity using Current-Reuse Technique for Broadband Applications

Pooria Sadeghpour[1] and Hamidreza Mirzaei[2,]*

1Electronic Branch, Islamic Azad University, Tehran, Iran
2 Young Researchers and Elite Club, Roudehen Branch, Islamic Azad University, Roudehen, Iran

ABSTRACT

A low noise amplifier is designed and simulated for the frequency range of 3.1 to 10.6 GHz using CMOS 0.18 μm technology. In this design there is a common source stage with an inductor in the source in order to reduce the amount of noise. The second stage is a structure to reuse the current in order to increase the gain and decrease the power consumption. Moreover, an NMOS transistor is used to improve the linearity of the proposed circuit. The proposed design is then simulated using the 0.18 μm CMOS technology in ADS software. The results show a noise level of less than 3dB and a flat gain of 14dB, also the IIP3 factor of the circuit is measured to be 0.5dBm which indicates the high degree of linearity in the circuit. The circuit power consumption is 23 mw.

* Corresponding author: *Hamidreza Mirzaei*

1. Introduction

In recent years, Electronics and Telecommunication systems, especially at high frequencies and in broadband applications, have made remarkable developments and as a result require circuits to transmit information at high speeds and low noise levels. Because the received signal, which may contain important and sensitive information, should be sent to the next level with high signal to noise ratio. As the size of transistors is diminished in CMOS technology and the cut off frequency is increased, the use of Broadband design has become more popular at a higher pace. The first stage of a receiver architecture is a low noise amplifier circuit, and has a significant role as it is the first receiver of the input signal. In [1] a common gate amplifier with current reused method is used for ultra wide band and low power consumption purposes. A common gate amplifier is located at the first floor of the input and compared to a common source amplifier, generates a signal -to-noise ratio independent of frequency. The current-reuse technique is used to reduce power losses along with acceptable power gain. Additionally, the shunt and series peaking is applied to a wide bandwidth. In [2], Distributed Amplifier (DA) circuit is used in order to achieve high gain. By dividing the transistors into smaller units and maintain a balanced distribution on the transmission lines, it can amplify the signal in good quality. In order to achieve low noise and power in this design, a two stage CMOS DA along with current-reuse technique and noise elimination is used. On the other hand, using parasitic capacitors (Cgd,Cgs) may reduce the bandwidth if used in a common source structure. But if parasitic capacitor adjustment is available at the input stage, parasitic effect can be ignored. A full integrated low voltage noise amplifier for low voltage and low power consumption is presented in [3]. This design is simulated in the process of CMOS 0.18µm by using the current-reuse technique and direct body bias method. The UWB LNA operates at very low voltage and power consumption since the direct body bias effectively reduces the threshold voltage. In this way, MOSFETs can operate at a lower bias voltage while maintaining gain linearity and noise factor. In current-reuse method in a PMOS cascade stage, an LNA is provided in [4] for the receiver of the UWB range using the 0.18 process. In order to achieve low power consumption, LNA uses the current-reuse technique in a PMOS cascade stage. The current-reuse technique can reduce power consumption while retaining high gain. However, because of using current-reuse technique in a second stage, LNA structure requires a DC bias and a separate bias resistance, hence additional noise and signal leakage will be generated. That is why the self-biasing circuit for the second stage is used. Noise elimination technique is applied to a low power ultra wideband low noise amplifier presented in [5]. This low noise amplifier includes a current-reuse cascade structure, a noise elimination technique, a common gate and output buffer structure, and a stagger-tuning technique combining the cascade of common gate and common bases that form the current-reuse structure and reduce the total power consumption by consuming the same DC current flow. In addition, a common gate structure that acts as an input amplifier stage, provides the impedance matching. A noise reduction structure is used in the structure of this amplifier, which reduces the amount of noise by reducing the noise source of the M_1 transistor. The stagger-tuning technique, by creation of oscillation points at high and low frequencies, as well as inter-class interfacing, will provide enough flat gain benefits as well as return loss. . L_2, L_3, C_b and other parasitic capacitors are used to obtain flat gain. The output stage is a buffer type of source follower that provides output impedance matching.

2. Proposed structure and Design Procedure

In this study, a two-stage structure is used to achieve the desired amplifier [6, 7]. In this scheme, the first stage is designed to reduce the noise and the second stage is used to increase the gain. Therefore, in a low noise amplifier design, a common source structure is used in the first stage and a structure similar to a cascade stage which is known as the current-reuse circuit is used in the second stage. This circuit is actually made of two common source stages with the difference that both stages have a common bias current.

The amplifier presented in [6] does not provide suitable linear performance and the IIP3 factor is relatively small. In this section a method to improve the amplifier linearity is presented. Linear low noise amplifier performance is determined by the nonlinearity of the transconductance and the linearity of the amplifier could be increased by lowering this factor.
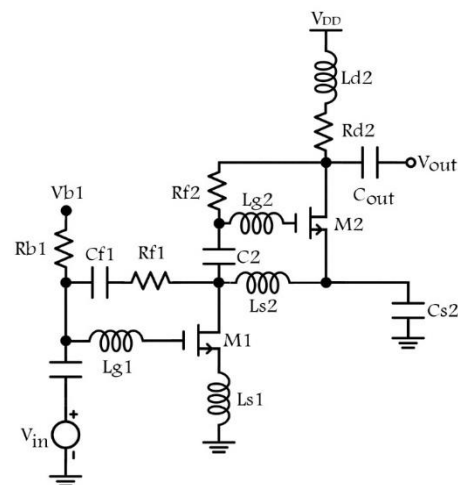

Fig.1. Low noise amplifier structure [6]

To improve the nonlinearity of the amplifier, the modified derivatives are used. In this method, using an NMOS transistor, it has been tried to improve linearity by reducing the equivalent value of g_m''. In this way, the acceptable value of IIP3 can be obtained [8, 9]. But two problems usually occur: the input matching collapses and the noise increases. To solve these problem, the input signal is not directly passed to the M_3 transistor and the gate of the transistor is joined to the source of the M_1 transistor. In order to reduce the bias sensitivity to bias voltage variations, it has been tried to achieve a very small g_m'' in a larger range instead of reading a zero g_m'' in a small interval. Further linearity enhancement of this amplifier will be possible by increasing the bias current. Here, using an auxiliary NMOS transistor, a low noise amplifier has been proposed in which

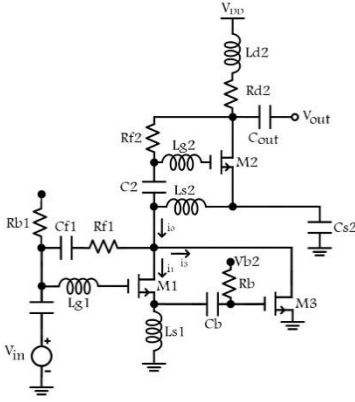the linearly has been improved and its circuit is shown in Fig. 2.

Fig.2. Low noise amplifier with applied linearity improving technique

3. Circuit analysis

To analyze how the mentioned circuit works, considering that the output current of the first stage is the total current of M_1 and M_3 transistor, we can say:
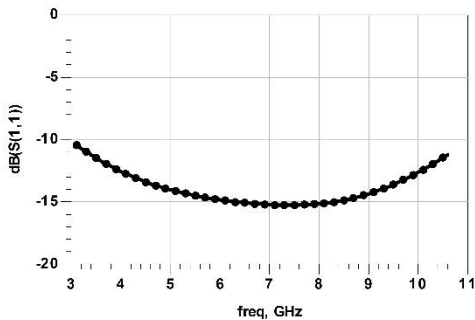
$$a)i_o = i_1 + i_3$$

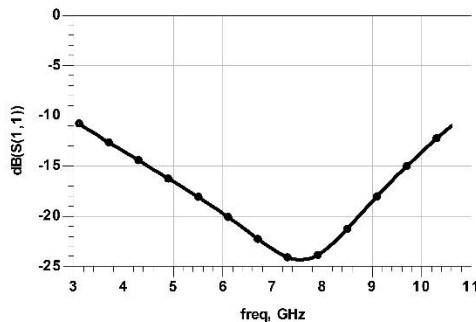$$b)i_1 = g_{1M1} v_{gs1} + g_{2M1} v_{gs1}^2 + g_{3M1} v_{gs1}^3$$

(2)

$$c)i_3 = g_{1M3} v_{gs3} + g_{2M3} v_{gs3}^2 + g_{3M3} v_{gs3}^3$$

(3)

It is clear that:

$$d)g_1 = \frac{\partial I_D}{\partial V_{GS}}, g_2 = \frac{1}{2}\frac{\partial^2 I_D}{\partial V_{GS}^2}, g_3 = \frac{1}{6}\frac{\partial^3 I_D}{\partial V_{GS}^2}$$

(4)

Also, the M_3 gate-source voltage can be written in terms of the M_1 gate-source voltage:

$$e)v_{gs3} = C_1 v_{gs1} + C_2 v_{gs1}^2 + C_3 v_{gs1}^3$$

(5)

The coefficients C1, C2, C3 are frequency dependent and can be obtained by simulation. In practice, with good approximation, C2 and C3 can be ignored. So we have:
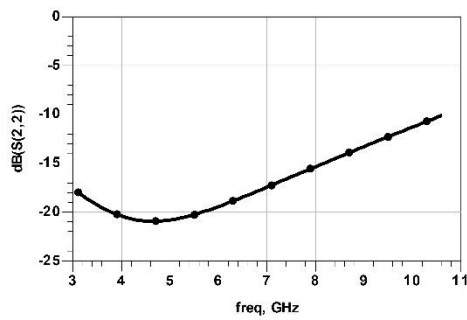
$$f)v_{gs3} \approx C_1 v_{gs1}$$

(6)

Clearly, the value of C1 is greater than zero. The output current is obtained by integrating the above relationships according to Vgs1.

$$g)i_o = (g_{1M1} + g_{1M3}C_1)v_{gs1} + (g_{2M1} + g_{2M3}C_1^2)v_{gs1}^2$$
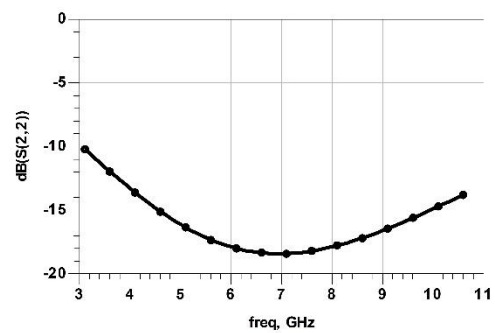$$+(g_{3M1} + g_{3M3}C_1^3)v_{gs1}^3$$

(7)

From (g) equation, we can see that if M_3 is biased so $g_{3M3} > 0$, since M_1 is biased in the strong inversion region and $g_{3M1} < 0$, (In fact the second derivative of the transconductance of the transistor M_1 is negative), nonlinearity of the third order of the amplifier should be reduced.

4. Simulation Results

Using the simulation of the circuit with the S-PARAMETER tool and setting its frequency range, the following results are obtained for the S parameters of the circuit.

(a)

(b)

Fig.3. S1,1 parameter simulation for 3-11 GHz frequency range a) before linearity improvement b)after linearity improvement

Fig. 3 and Fig. 4 show the simulated values of the parameter S11 and S22 (return loss in the input and output) in the entire frequency range of simulation. the linearity improvement technique results in a value less than -10dB for S1,1, and less than -15dB for S2,2 which is acceptable based on previous studies.
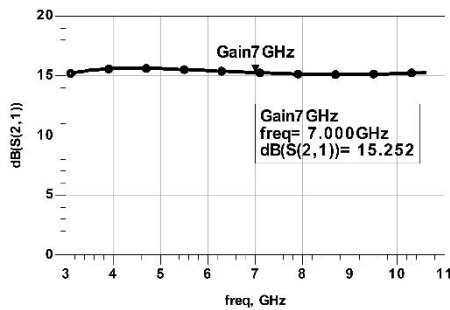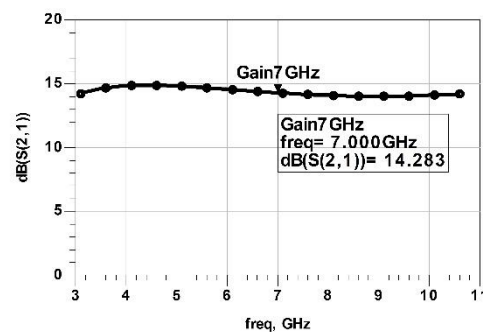
(a)　　　　　　　　　　　　　　(b)

Fig.4. S2,2 parameter simulation for 3-11 GHz frequency range a) before linearity improvement b)after linearity improvement

As shown in Fig. 5, the value of the S21 parameter (gain) of the circuit with a linearity improvement technique has a value greater then 14dB and deviations of less than 1 dB over the entire frequency range.
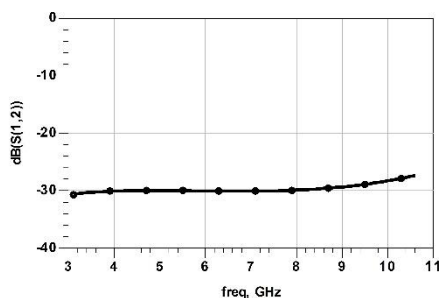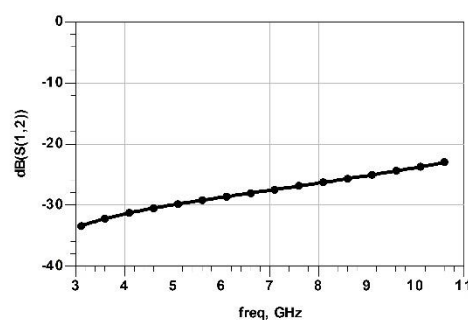

(a)　　　　　　　　　　　　　　(b)

Fig.5. S2,1 parameter (gain) simulation for 3-11 GHz frequency range a) before linearity improvement b)after linearity improvement

As seen in the Fig. 6, the value of the S12 parameter of the circuit which is the return gain (output to input), has a value of less than -23dB over the entire frequency range, indicating a suitable return isolation of the circuit.
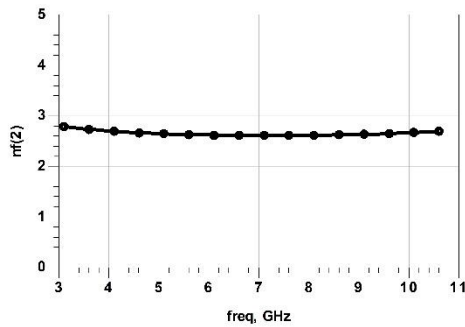

(a)　　　　　　　　　　　　　　(b)

Fig.6. S1,2 parameter (return gain) simulation for 3-11 GHz frequency range a) before linearity improvement b)after linearity improvement

The result of noise figure (NF) simulation of low noise amplifier using linearity improvement is investigated in the next step. By activating the calculation of noise in the above-mentioned S-parameter tool, the circuit noise figure

is obtained as follows. According to Fig. 7 the noise figure (NF) of the circuit is less than 3dB over the desired frequency range, which indicates an acceptable noise level.
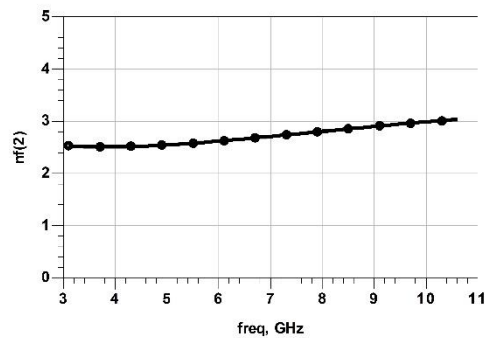
(a)   (b)

Fig.7. Noise Figure (NF) simulation for 3-11 GHz frequency range a) before linearity improvement b) after linearity improvement

By performing a DC circuit analysis and calculating the product of the supply voltage and bias voltage in the current drawn from them, the power consumption of the two circuit are obtained and compared as follows. According to the obtained result, the power consumption of the designed circuit is 23.43mw which was predictable due to usage of linearity improvement unit in the proposed circuit.

Eqn Power_diss= -(DC.SRC1.i* DC.Vdd)-(DC.SRC2.i* DC.Vb)

freq	Power_diss
0.0000 Hz	23.43 m

Fig.9. Power consumption calculation of the low noise amplifier using linearity improvement technique

Another important factor in the LNA specification is the 1dB compression point. Using the circuit simulation with the HARMOUNIC BALANCE tool, the results for the (P_{1-dB}) of the circuit compression point before applying the linearity improvement technique are shown in fig.10.

Eqn Power_diss= -(DC.SRC1.i* DC.Vdd)-(DC.SRC2.i* DC.Vb)

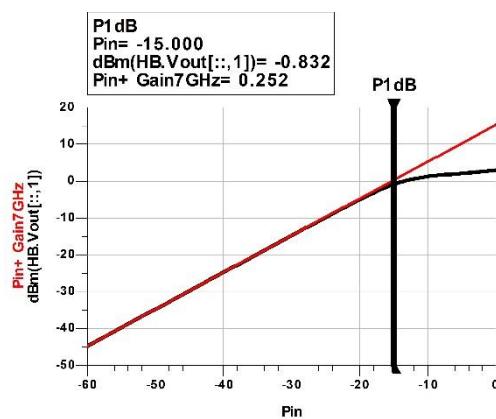| freq	Power_diss
0.0000 Hz	12.97 m

Fig.8. Power consumption calculation of the low noise amplifier before linearity improvement
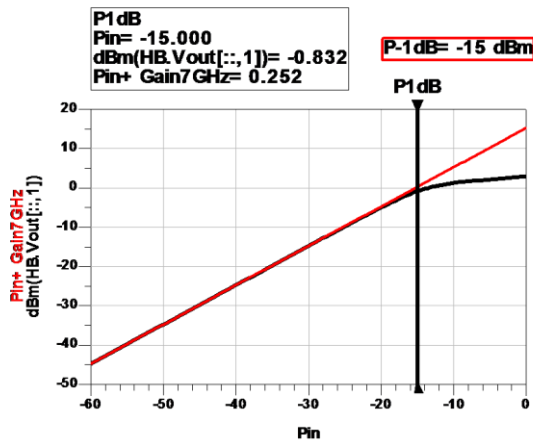
(a)   (b)

Fig.10. The results for the (P_{1-dB}) of the circuit before applying the linearity improvement technique.

By definition, P_{1-dB} is the amount of power input in which the amplifier gain decreases by 1dB. Given the curve shown in Fig. 11, the simulated P_{1-dB} for the low noise amplifier after applying the linearity improvement technique is 9.5dBm, which shows 5.5dB improvement over the original design.
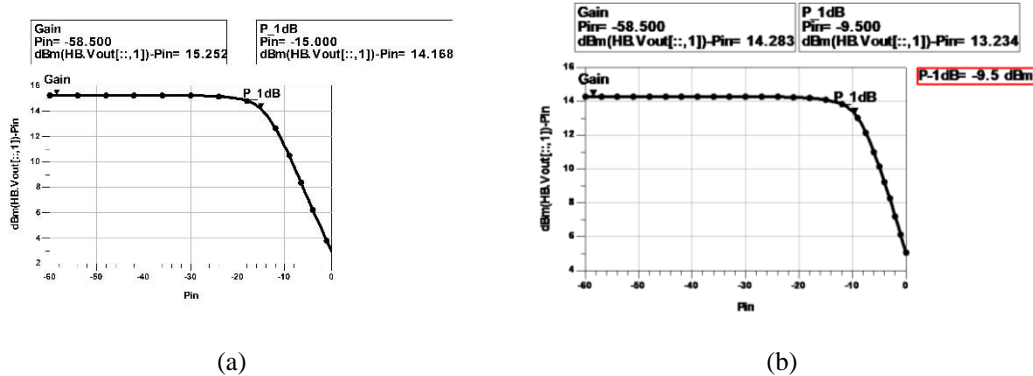
(a)   (b)

Fig.11. The results for the (P_{1-dB}) of the

circuit after applying the linearity improvement technique.

In the following, the proposed low noise amplifier IIP3 is calculated. Using the simulation of the circuit with the

HARMUNIC BALANCE tool and adjusting its parameters, the results are obtained for the third-order intersection point, IIP3, of the circuit.

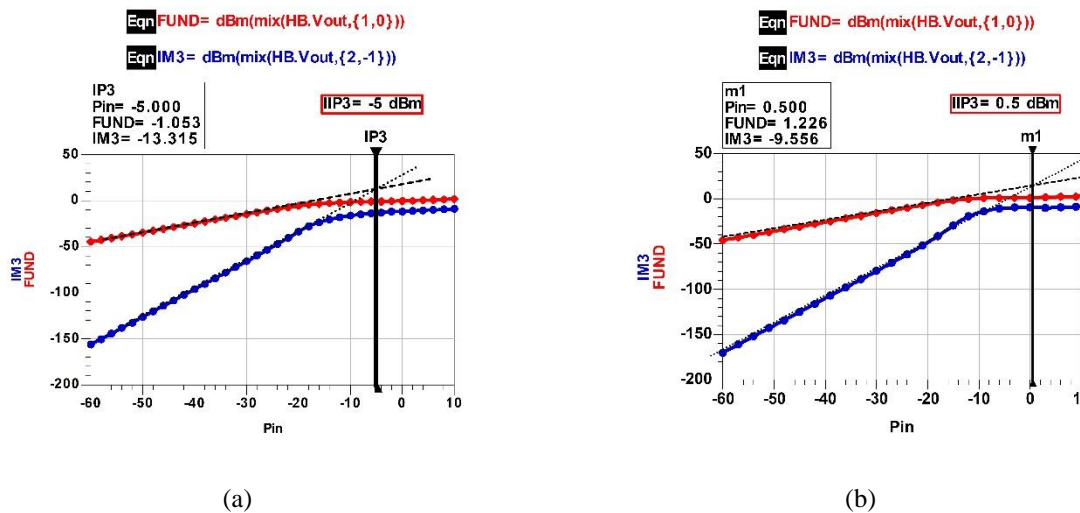(a)   (b)

Fig.12. Low noise amplifier IIP3 calculation a) original design b)using linearity improvement technique

By definition, IIP3 is the amount of input power in which the main output and harmonic power curves collide. With respect to the above curve, the IIP3 value of the low noise amplifier by applying a linearity improvement technique is approximated by 0.5dBm, which is a rather high value based on previous studies and represents a 5.5dB improvement compared to the original circuit.

In final step low noise amplifier circuit stability diagram with linearity improvement technique is illustrated in Fig.13. As can be seen, the coefficient K is greater than 1, and therefore the circuit is stable throughout the entire frequency range of 3-11 GHz .
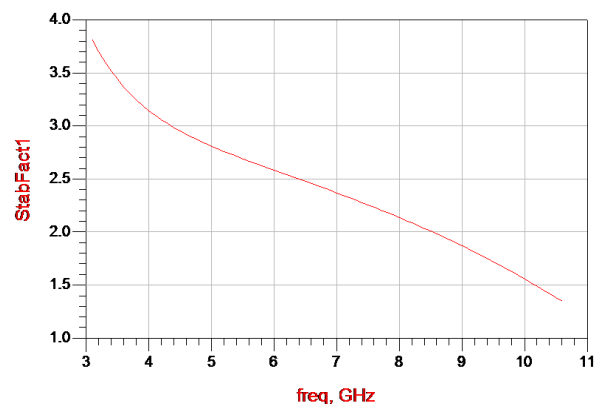

Fig.13. Low noise amplifier circuit stability diagram with linearity improving technique

The results obtained from the simulation of the original circuit and the improved design are summarized in Table. 1.

Table.1. The comparison between original circuit and the improved design

parameter	Original circuit simulation results	Proposed circuit simulation results using recovery technique for IIP3
Technology	0.18 μm CMOS	0.18 μm CMOS
Power Supply	1.8 V	1.8 V
Frequency range	3.1 GHz ~ 10.6 GHz	3.1 GHz ~ 10.6 GHz
NF	< 2.8 dB	< 3 dB
gain: S21	> 15.1 dB	> 14 dB
Input return loss: S11	< -10.4 dB	< -10.7 dB
Output return loss: S22	< -10.1 dB	< -10.2 dB
Reverse isolation: S12	< -27.3 dB	< -23 dB
Power consumption	12.9 mW	23.4 mW
P-1dB	-15 dBm	-9.5 dBm
IIP3	-5 dBm	0.5 dBm

5. Conclusions

In this study, a wideband low noise amplifier is offered in the 3.1 to 10.6 GHz bandwidth in CMOS 0.18μm technology. In this design, a structure similar to a cascade stage which is known as current-reuse technique is used in the second stage. In the presented circuit, the first stage is designed in order to reduce the noise figure and the second stage is used to increase the gain and reduce power consumption. Then, in a new circuit, an auxiliary NMOS transistor is used to improve the first stage linearity. The performance of the low noise amplifier is simulated using the CMOS 0.18μm technology in ADS software and the simulation results indicate a noise figure of less 3dB and an input return loss of less than -10dB, 0.5dBm of linearity and 23.4mw power consumption in the 3.1 to 10.6 GHz frequency range.

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