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Optimization of carbon nanotube field-effect transistors (CNTFET) and compare them to CMOS silicon

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ABSTRACT

In this paper, a brief review of CNT carbon nanotube transistors will be explained and then the optimization methods will be discussed. Details of AC and DC transistor CNFET and Characteristics of CNFET at high temperature also shows that unlike MOSFET flo below the threshold for this type of component temperature is reduced, thus using CNFET at high temperatures can be more quickly and less leakage current is achieved. Processes for the synthesis of CNT are not complete, a subject of controversy in the field fluctuations of density in CNT growth, as well as an analysis of the credit CNFET because sway density of CNT could lead to complete failure CNFET, so to evaluate it, and we later CNFET applications in comparison with CMOS logic circuits using the latest research, we'll CNFET.

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Introduction

With the passage of time and advancement of science and technology daily human need to learn and speed of processing them into shorts and storage is increasingly high. Gordon Moore, Intel's senior vice president in 1965, offered a theory that the number of transistors on a chip every 18 months doubled the size it used to be Nsrf. These concerns led to shrinking the size of transistors that can be small. Moore theory must be built according to the thickness of the oxide transistors in them less of a nano-meters and able to maintain their performance. CNFET was built in 1995 for the first time [1]. Field-effect transistor using nanotubes are one-dimensional semiconductor. To make a one-dimensional carbon nanotube is a cylinder only need to have the ease of the process of making one-dimensional nanotubes makes up as a replacement for transistors are promising. Extensive research efforts to take advantage of carbon nanotube field-effect transistors (CNFETs) as an alternative or complement to future semiconductor components due to high Therapy, low defect structure and exceptional electrical characteristics, such as the transfer of quasi-ballistic (no scattering channels ballistic properties) makes them suitable for high speed and high performance circuits are designed. CNFET your high superior performance and the most advanced pieces of silicon have shown. It is expected that the ideal technology CNFET (in the sense that all carbon nanotubes are semiconductors similar thickness as well as quite a good position to Traznd) times faster than silicon CMOS, while the similar energy consumption [2].Expect them as one of the most promising technologies that may one day old pieces shall pass CMOS. CNT electronics industry based on not only a lot of advantages to maintain existing silicon technology, but this piece a lot of problems that may prevent the achievement CMOS into very small pieces resolve 3. So far CNFET for the advancement of research on the structure of the segments and segment performance have been tested, but the theory CNT transistor technology is still in its infancy and it has not yet fully formation [4].

1. Carbon nanotubes (CNT)

Carbon nanotubes are graphene bands that come in the form of pipes. Due to its flat graphite sp2 connections has a hexagonal structure, the carbon nanotubes at the molecular level, the structure of hexagons shown in (Figure 1). Iijima first observed in 1991 that carbon nanotubes contain a kind of molecules with unique properties of mechanical, thermal and electrical. Some of these features is a close link between carbon nanotubes and graphite, and the rest of the one-dimensional emanated them [5]. Figure 1 microscopic view of a carbon nanotube, as described to illustrate

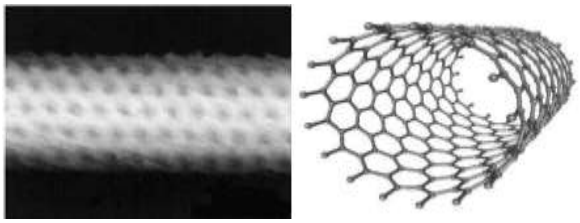


Figure 1. SEM image of a carbon nanotube

Carbon nanotubes have different applications in different conditions. These applications use them as a source of electron field emission devices, interconnections and FET devices on bag included [6]. CNT in the form (3), a layer of carbon atoms, of which one wall carbon nanotubes (SWCNT) are called. Multi-wall carbon nanotubes (MWCNT) with the center of SWCNT of different thicknesses, respectively. Thickness SWCNT could be as small nm 0.4. Normal thickness between 0.7 nm 3 in change [6]. Therefore, it is important that the energy gap CNT thickness indicates the pipe connection. SWCNT binding energy gap is expressed as follows [6]:

(۱)

$$D_{CNT} = \frac{\sqrt{3}a_0}{\Pi}\sqrt{n^2 + m^2 + mn}$$

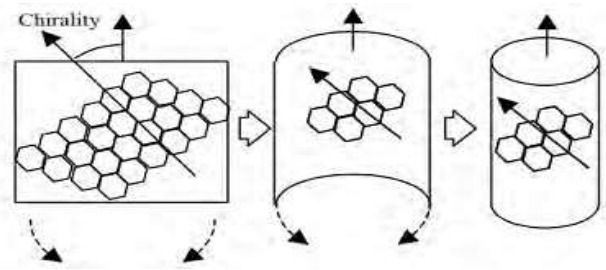


Figure 2: Chyralyty a CNT [6]

Where E is the band gap, γ0 are carbon-carbon (nm) and d is the thickness of the nanotube. The band gap d is longer than the nanotubes are conductive. It can be done if the curvature of the tube-like graphene sheet will be reduced. Electrical carriers in the CNT dispersion is affected as a result of network defects and vibrations occur and eventually their resistance, this is also happening in many other materials. CNT one-dimensional nature and strong bond covalently they strongly influence the process. Semiconductor nanotubes under the influence of their behavior Chyralyty. In a carbon nanotube and graphene ribbons Chyralyty angular difference between the orientation of the resulting nanotube axis (Fig. 2) of CNT semiconductor field-effect transistors is the main reason for trying to make (CNFET).

2. Performance CNFET

Carbon nanotube field-effect transistor (CNTFET) of the CNT channel semiconductor is used. A single-walled CNT (SWCNT) only contains a simple process of making this piece of pipe and replacing it with MOSFET is promising. A SWCNT depending on the angle position of the atoms in the direction of the tube, it can act as both a conductor and a semiconductor.

This vector is called Chyralyty and a pair of integers (m,n) show. A simple way to determine whether a metal or semiconducting CNT is that its index (m, n) 's. When the metal tubes that n = m or n-m=3i, which in this case i is an integer. Otherwise, the semiconductor tube. CNT thickness can be calculated using the following equation [6].

$$E_{gap} = 2Y_{0c-c} / d \qquad (2)$$

Where m 0.142 = a0 subatomic distance between adjacent carbon atoms, and the atoms it. Properties IV, CNFET MOSFE is similar. The threshold voltage is the voltage required to turn on the transistor. Internal CNT channel threshold voltage can be in first place, while half of the bond gap, the thickness is reversed. CNFET like a traditional piece of silicon four terminals. As Figure 3 shows, semiconductor nanotubes without impurities under the gate to the channel region, while parts that are strictly between the gate and source-drain by the gross CNT are that allow the formation of a low resistance in the on state. When the gate potential increases for electrostatic piece through the gate on and off [6]. Voltage gate to source the reference current threshold voltage of the transistor as the same is now considered to be a different Chyralyty. CNFET the unique opportunity to control the threshold voltage by changing the thickness of the CNT cause Chyralyty vector

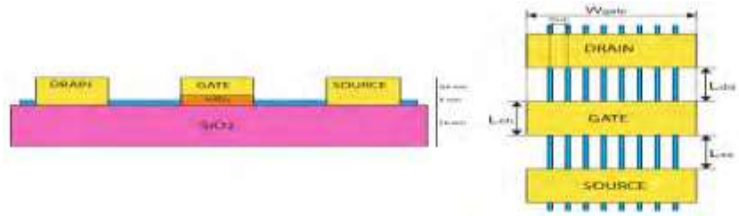


Fig. 3 shows the outline of a transistor CNT. (Left) facing to the right) Top view [2]

SWCNT synthesis process to produce the desired Chyralyty structure (m, n) in the R Kumar Sinha et al (2012) [6] have been proposed. CNFET are clearly due to ballistic transport canal, convenient for the gate dielectric high-k material physics and new pieces are interesting. Although so far all actions performed on CNFET focus on the characteristics of DC, but AC characteristics technical characteristics are appropriate. It is predicted theoretically that, ballistic system operates short nanotubes and quantum capacity, both must have the ability to increase the THz range [6].

3. The method of performance optimization CNFET

A. Increasing the efficiency of the gate voltage set for channels SWCNT

Another important way to improve performance by increasing the efficiency of regulation CNFET gate voltage is SWCNT channels. Currently, there are three main ways to increase the efficiency of the gate set.

1. **The use of high-gate structure**

The solution to this problem is to produce a high gate CNTFET For this purpose, source and drain electrodes on both ends of the SWCNT production. And then an insulator composed of SiH4 and O2 is deposited by CVD on SWCNT and finally a Ti or Al electrodes on the channel cover SWCNT. This leads to a high gate structure effectively increase the gate bias effect of regulation

2. **Reducing the thickness of gate insulator**

For this method to be a natural oxide layer on the Al2O3 on Al electrode used as a gate insulator or by depositing SWCNT HFO2 the function of DNA with a sludge technique, atomic layer ALD)), CNFET very thin gate insulation High- high k produced

B. Reducing the contact resistance between the SWCNT and metal electrodes

SWCNT when placed on metal electrodes, high contact resistance between SWCNT and electrodes lowers performance piece. Many methods have been tested to reduce contact resistance, among which are: (1) heating at high temperature; (2) the independent semiconductor SWCNT between source and drain electrodes and Upgrade with CVD; (3) the appropriate metal as electrode contacts, research shows, Au with SWCNT contacts proper and valid form. Pd and semiconductor SWCNT can also contact form ohmic contact resistance is significantly reduced; (4) nano-ultrasound welding techniques and a new approach for making hard contact with low resistance between both electrodes of semiconductor and metallic SWCNT

C. Shortening the length of SWCNT

When MWCNT channel is long (more than a few micrometers), carriers will be published in the transport process that it reduces the carrier Therapy. Seidel et al. (2005), [8] a channel length nm 18 reported CNTFET. They hydrogen silsesquioxane) HSQ) was used to successfully channel are very small (less than ten nanometers) produced. However, it should be noted that the effect of improving the technique when the channel length of SWCNT smaller than the free path of carriers is reduced, because the transfer of ballistic carriers in SWCNT and Therapy piece mainly by calling feature at this time is determined the

E. Optimized device structure

Research Lin et al. (2005) [9] showed that the use of a double-gate CNTFET yield followed.
In the study, Chen and colleagues (2007) [3] CNTFET with channel multiplexing design in which an array of SWCNT parallel to weld nano metal electrodes are placed so as to channel CNTFET act, which resulted in higher interest , reliability better and more useful than single-channel CNTFET was. In particular, a gate CNTFET around the axis (Fig. 4) were predicted to have the highest performance piece in which the CNT by a thin insulating layer was coated with a thickness of approximately nm 1. Performance wonderful piece increased due to the impact of effective regulation of the gate for the CNTFET**.**

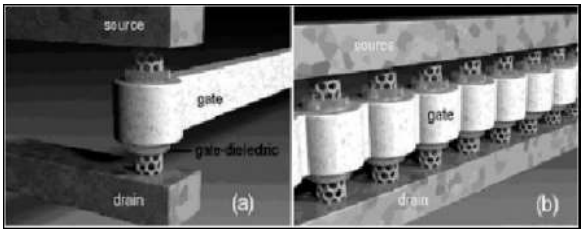


Figure 4: CNTFET gate around the axis

4. AC and DC transistor characteristics CNTFET:

Advances in semiconductor tube of carbon nanotube field-effect transistors with high performance has been remarkable. For example, in just 4 years trans conductance component gm=did/dv by more than three factors: The size of a couple of ns to μs few microseconds in each tube is improved [10]. Considering the small channel width of the transistor (the diameter of a nanotube is near to nm) and ignore the problems related to large-scale, may be instantaneous flow by an array of pipes (tubes) form. Highlights the important reasons for the electrical properties of carbon nanotubes there. The energy gap between these bands one-dimensional (1D) due to the gradual (quantization) surrounding the tubes, allowing one-dimensional transmission at room temperature is ideal. Distribution of nanotubes within the limited space available phase is suppressed, the consequences for the distribution and movement of more than a few hundred nanometers ballistic properties are protected. [10] Another major advantage Nano the tubes, wires or plates, for example silicon atom chain that hung in there and periodically scattering surface hardness limiting factors for the performance CNFET that it is very, very thin piece of body normal is different. It also refers to the fact that carbon nanotubes can easily High-k material for the gate as insulation than conventional materials. [10] All the above-mentioned tests aiming at the performance of DC, FET is of nanotubes. Also recently, scientists have begun to explore the properties of AC, CNFET of them. While higher value component trans conductance (gm) of the above suggests that nanotubes with the characteristics of high-frequency components are the best. And it tentatively to bring out the characteristics of the AC, CNFET valid challenged. Using a

new technique to measure recently shown that FET pipe (tube FETs) can at least signal attenuation frequency MHz 600 without any work. [11]

5. CNTFET properties at high temperatures

A: CNTFET flow under thermal fluctuations

In this section, a new compact model to study CNFET saturation and approximate delay the release of high temperature tested. In MOSFET drain current and temperature dependence of threshold voltage variation with temperature stems Therapy and although CNFET dependence of the Fermi surface often (Fermi) and changes in temperature stems majority carrier concentration. The density model (compact) a carbon nanotube diameter and length nm 1.7 nm 18 with a layer of oxide layers ZRo2 as a simulation. Formula (1) for a chain of one-dimensional density semiconductor

$$D(E) = 2\times 2\times \frac{1}{L}\sum_{\Delta k_t}\sigma[E-E'(\Delta k_t)] = \quad \textbf{(3)}$$

$$D_0 \frac{|E|}{\sqrt{E^2-(E_G/2)^2}}\Theta(|E|-E_G/2)$$

D0: metal chain from the DOS, (θx is a step function for 0 <X equal to 1, otherwise it is equal to zero, EG band gap of the CNT. The band gap is equal to:

$$E_G = \frac{a2a_{acc}|t|}{d} \approx \frac{0.8eV}{d} \quad \textbf{(4)}$$

Each chain in leading edge high production capacity of singularities, as in Figure 1 is shown:

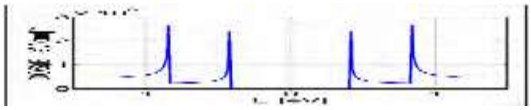


Figure (5): DOS (13,0) CENT calculated using equation number one [13] to calculate the flow rate in CNFET this, we are the majority carrier concentration, + nL work began. + NL formula is:

$$n_L^+ = D_0\int_0^\infty \frac{|E|}{\sqrt{E^2-(E_G/2)^2}}\left(\frac{1}{1+e^{(E-E_F)/k_BT_L}}\right)d_E \quad \textbf{(5)}$$

$$= \frac{N_{CN}}{2}\int_0^\infty \frac{(\xi+\xi_G/2)}{\sqrt{\xi^2+\xi_G}}\left(\frac{1}{1+e^{\xi-\eta_F}}\right)d\xi$$

∩F in the above formula is a function of gate voltage and its application are as follows:

$$V_D = \frac{(V_G-V_T)}{K_BT_L/q} + \frac{q^2N_{CN}}{2K_BT_LC_{ins}}\{F(\eta_F)-F(\eta_F-U_D)\} \quad \textbf{(6)}$$

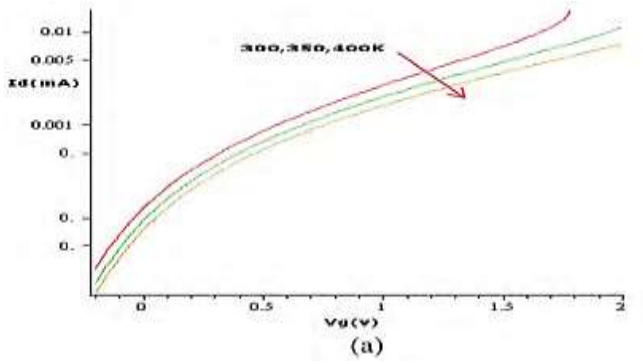
We have a quadratic function of (F) ηF have used the following

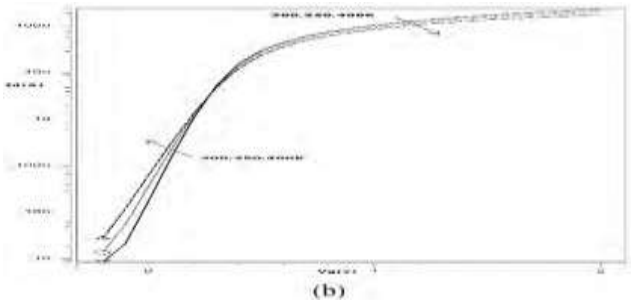
$$F(\eta_F) = \alpha\eta_F^2 - \beta\eta_F + \gamma \quad \textbf{(7)}$$

Where all coefficients in the formula (6) are a function of VD. As a carbon nanotube channel was substantially one-dimensional materials with respect to the ratio analysis, so the current between source and drain using Lambda formula of (Landauer) is calculated: $I_D = \frac{2qk_BT_L}{h}\{F(\eta_F)-F(\eta_F-U_D)\}$ **(8)**

CNTFET drain current modeling in front of the gate voltage source (V) for different values of the temperature in the drain to source voltage in Figure 0.9 (a) is shown. In this form of drain current is plotted on a logarithmic, where the gate voltage is linearly the graph more meaningful values of leakage current, for example, drain current when the gate voltage is zero gives us. We Hspice simulation and 32nm technology was used for the bulk MOSFET in Figure (b) The results of drain current density changes with temperature were compared with the CNFET [13].

As shown in the pictures. When the temperature (T) from 300 Kelvin to 400 Kelvin increases the leakage current of 60nA and 90nA for CNFET reduced, but the MOSFET, nm 32 nA 63 to increase the flow of nA 17 decreases. Reduce the leakage current at high temperature transistors CNFET are good for high heat applications make





(b)

6. variability and reliability in the presence of fluctuations in the density of the CNT CNTFET

A. Fluctuations CNT synthesis process

The process of the synthesis of CNT, are far from perfection. CNT synthesis process made major advances in the field, however, accurate control Chyralyty (angular position of the atoms in the direction of the tube) problem is not solved. Chyralyty responsible for the random distribution of the thickness of the CNT. Yvnd gap thickness fluctuations strongly affect CNT (CNT thickness is proportional to the energy gap upside down) and cause fluctuations in the threshold voltage is a CNFET. Another challenge associated with fluctuations in the density of the CNT [7]. We need to increase the density of the CNT. The average density of the CNT is calculated CNTs.µ50 -10 minimum density for logic circuits need CNTs.µm 250. There are metallic CNT (m-CNTs) in the semiconductor CNT also considered an obstacle. The process according to the synthesis of CNT, 3.1 and 3.2 of semiconductors are made of metallic CNTs. In order to reduce the proportion of m-CNTs can be used in different processes. With regard to the development of improved methods for CNT, a percentage between 96% to 090/0 s-CNT have been successful. However, progress in (% of m-CNT for digital circuits VLSI scale is not enough. For the circuits VLSI CNFET leakage, noise and oscillation, they should be deferred to less than 0.01% reduction in the amount of m-CNTs [2]. The third option to remove m-CNTs after CNT growth process is at work. Techniques available to remove m-CNT, single-device electrical failure (SDB), and remove the gas phase removal techniques based on chemical reactions to remove or metallic CNT compatible with VLSI (VMR) to be included [2]. In short, we can conclude techniques available to remove m-CNT and are not compatible with VLSI but must be paid a high price for it. Therefore, optimizing the removal of m-CNT and circuit design necessary for the provision of digital logic circuit uses strong, that CNFET. It is worth noting that the results of the removal of m-CNTs are also causes fluctuations in the density of the CNT. In addition, m-CNT removal techniques are not perfect. They eliminate the unwanted number of s-CNTs and also reduce the density CNTs

(B) credit analysis

Carmen et al. (2012). [2] In short, a way to evaluate the effect of density fluctuations on the technology offered CNFET. In this study, the process of removing m-CNT was considered ideal. This means that all transistors are provided in the m-CNTs have been removed, while all of them have remained intact. This hypothesis is optimistic, because in reality Ida removal techniques are not ideal, the number of m-CNTs after removing the -m CNT remain and some randomly removed during the process. Although nearly 100% excluding m-CNT is achievable, but non-negligible fracture s-CNTs usually 10% -40%) have been destroyed. As a result, fluctuations in the density increases, and above all CNFET may be damaged. The fact is the key influence on the validity of CNT technology. In this section, two types of failure in CNFET would consider.

1. Very bad defeat: CNFET in a transistor-like behavior fails (open or short) or decadent behavior shows.
2. Parametric failures: CNFET transistor acts as a boundary but some situations does not cause design requirements.

An open fracture occurs when no CNT to connect the source and drain connections there and it is achieved when all of CNT are deleted. On the other hand, the leading m-CNTs in the transistor makes the connection because they lack control over current conduction by the gate. Finally, the presence of m-CNTs in the s-CNTs may be tube-like behavior of transistors and n-CNFET decadent. In short, failures can be very bad: open transistor-like behavior, are short and degenerate classification

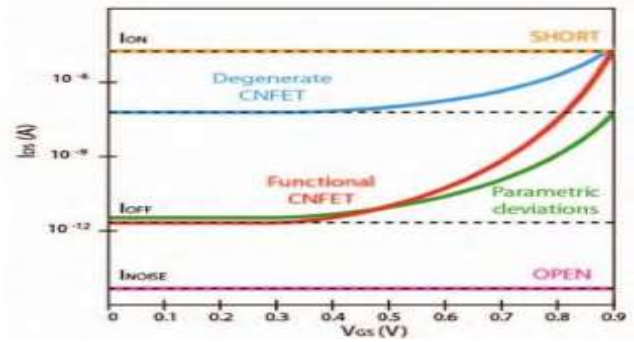


Figure 6: Breakdown of the poor, parametric and characterization CNFET efficient [2]

Note that by increasing the number of CNT per transistor and reducing pm (probably metallic, semiconductor and), the probability of failure (pf) is also reduced. When Prophet obviously an ideal process to remove m-CNT into account Y r y m, SC7 (% 5 = and pm% 0 = psR [semiconductor possibility of) the minimum pf and SC3 (% 40 = and psR% 33 = pm)Highest pf (worst) is introduced. Therefore Carmen et al. (2012) [2] showed that the low probability of m-CNTs (% 5 = TM) are all efficient transistors, while the probability of m-

CNT (= TM% 33), 3.2% and 6.2% respectively transistors CNFETs 32nm and 16nm are inefficient

Table 1: Percentage of efficient and inefficient CNFETs

	Wgate=32nm		Wgate=16nm	
Tm	5%	33%	5%	0.033
Very bad	0%	0%	0%	0.4%
Parametric failure	0%	3.2%	0%	6.2%
Efficient CNTs	100 %	96.8 %	100 %	93.4 %

7. Comparison with MOSFET and use CNTFET

A logic circuits based on CNTFET

FINFET promising alternative to silicon transistors for low-power circuit design with high performance due to its ballistic characteristics of the carrier off its low. The results of this study show that a combination of logic gates design uses dual triple and proper way for large-scale integrated circuits design, low power consumption and high performance is CNTFET. Current density, the speed of the piece, propagation delay through the gate and save 57% power can be set using a conventional CMOS Mbypvlar CNTFET obtained. Universal cells that have been transformed dynamism, the possibility of dense circuits, systematic and highly flexible platform-based system on chip layout is created in the [6].

B. Digital to analog converter (DAC)

Now is the right time to introduce CNT FET technology regime DAC converter and the performance is by CNFET. In this section, a digital to analog converter (DAC) current command GSample.s-1 bit-10 on CNFET technology is provided. All digital to analog converter building blocks are made by CNFET. Supply voltages of less than one ampere. The design of the structure has been fabricated and DAC binary level. The building blocks of CNT technology used by leading to lower voltage jumps, clock, and power consumption is Tvgzr.

Simulation results show that the artificial free dynamic range (SFDR) of 62dB at Nyquist rate of the input sampling frequency equal to -1 GS.s is 250 MS.s. The comparison between the DAC and DAC command Si technology with CNFET the command indicates that the voltage jumps in energy, power, and time clock T v gzr meeting CNFET are very low, for example, to command the 10-bit DAC, voltage jumps, 2.64pV. S, while it is 0.13 pV.S [14].

8:conclusion

According to numerous studies that CNFET face and optimization methods to solve the shortcomings of the challenge and despite the many advantages that these parts (CNFETs) compared to MOSFET are still a long way to industrial applications CNFET there, While still unwanted growth during manufacture of metal tubes CNT are also considered as a challenge and a negative impact on latency, power and performance are CNT-based circuits. In this regard, the results of theoretical and experimental prospect clearly shows us that although the scope of discussion, dialogue and research also needs broader whatever.

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