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Evaluation and Comparison of CMOS logic circuits with CNTFET

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ABSTRACT

In this paper, a comparison between CMOS and MOSFET base circuits HSPICE is done with software. 0.13μ CMOS transistor model for simulation and CNTFET Model of Stanford University used. In simulations amounts of power, circuit delay and PDP is calculated and these values were compared at the end. And tried to CNTFET applications of transistors in circuit design, including memory and logic circuits Ternary be expressed.

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Introduction

CNTFET transistors due to their small size and properties of polarity change is expected to be the best alternative for CMOS transistors [1]. Monopolar and bipolar transistors are made in the two samples (Ambipolar) [2]. Ambipolar type because of the variability of the electrical signal polarity, is suitable for the implementation of programmable logic circuits. But now CNTFET transistors are unstable [3]. After making the transistor to give a good answer in some cases, but sometimes, it's not good properties and does not answer well. Even with pessimistic assumptions CNTFET nano electronics can be achieved remarkable performance compared to silicon technology. Electronic conductivity and thermal conductivity of nanotubes good or even better than precious metals. The mechanical strength of carbon nanotubes is very high. The benefits of a good system of CNT-based electronic devices is expected, However, many of the challenges of technology and materials for them. Controlled growth of CNT still needs to dominate. In connection to the source/drain on CNT ideal mechanism for better estimating the performance of the device is required. Replacing the metal connection joint CNT Source/Body with a very high doped source/drain (ohmic like) can improve the device performance.

2. CNTFET

In 1991, for first time Sumio Iijima observed carbon nanotubes [4]. A carbon nanotube in CNTFET is placed between drain and source of the transistor, Fig.1 . This model is based on Stanford CNTFET model [5].

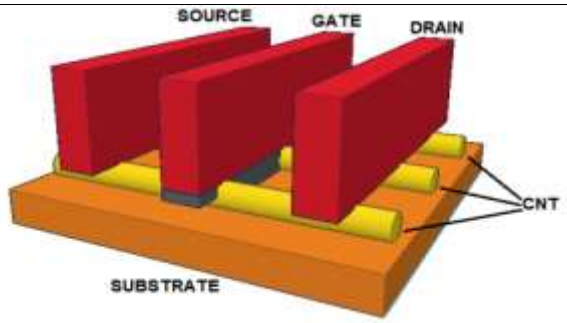


Figure 1: CNTFET transistor

CNTFET have some Features, like: low cost and high degree of reliability. When gate lengths are scaled down in nanoscales, it results in various crucial challenges and reliability issues that may reduce its potential for energy efficient applications [6]. Typical electrical properties of CNTFETs like higher speed, higher dielectric constant and stability provides good characteristics than Silicon based MOSFETs [7]. There are different classifications for CNTFET structures, like: 1. Multi Wall CNT (MWCNT): Each CNT contains several hollow cylinders of carbon atoms nested inside each other, 2. Single Wall CNT (SWCNT): that is made of just a single layer of carbon atoms. These are most common type of CNTFET. Fig.2 represents different types of CNTFET.

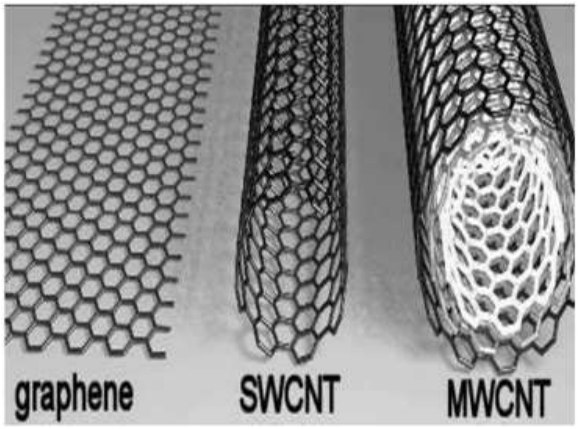


Figure 2: Types of CNTFET transistors

CNTs have a diameter of a few nanometers and it's between 0.7nm to 0.3nm in single walled CNT [8]. The diameter of the CNT is directly related to the carbon-carbon distance (a_0) and the chiral vectors (n,m) [9].

$$D_{CNT} = \frac{\sqrt{3}a_0}{\pi}\sqrt{n^2 + m^2 + nm} \quad (1)$$

In Ao Teng thesis [13], The physical properties of CNTs have been provided and summarized in Table 1.

Table1: Structural Parameters for (n, m) CNTS where n, m, t1, t2 are integers.

Symbol	Name	Formula	Value
a	Lattice constant	$a = \sqrt{3}a_{cc} \approx 2.46\text{Å}$	$a_{cc} = 1.42\text{Å}$
a_1, a_2	Basic vectors	$\left(\frac{\sqrt{3}}{2}; \frac{1}{2}\right)a, \left(\frac{\sqrt{3}}{2}; -\frac{1}{2}\right)a$	-
b_1, b_2	Reciprocal-lattice vectors	$\left(\frac{1}{\sqrt{3}}; 1\right)\frac{2\pi}{a}, \left(\frac{1}{\sqrt{3}}; -1\right)\frac{2\pi}{a}$	-
C_h	Chiral vector	$C_h = na_1 + ma_2 \equiv (n,m)$	$(0 \le \lvert m\rvert) \le n$
d_t	Tube diameter	$d_t = \frac{\lvert C_h\rvert}{\pi} = \frac{a}{\pi}\sqrt{n^2 + nm + m^2}$	-
θ	Chiral angle	$\sin\theta = \frac{\sqrt{3}m}{2\sqrt{n^2 + nm + m^2}}$ $\cos\theta = \frac{2n + m}{2\sqrt{n^2 + nm + m^2}}$	$\left(0 \le \lvert\theta\rvert \le \frac{\pi}{6}\right)$ $\tan\theta = \frac{\sqrt{3}m}{2n + m}$
T	Translational vector	$T = t_1a_1 + t_2a_2 \equiv (t_1, t_2)$ $t_1 = \frac{2m + n}{N_R}, t_2 = -\frac{2n + m}{N_R}$	$gcd(t_1, t_2) = 1^a$ $N_R = \gcd(2n + m, 2m + n)^a$
N_C	Number of C atoms per unit cell	$N_C = \frac{4(n^2 + nm + m^2)}{N_R}$	-

*gcd(n,m) denotes the greatest common divisor of the two integers n and m.

3. Simulation of CMOS Circuits

3.1. Inverter simulation with CMOS

To make the simulation results can be compared with CNTFET model should achieve results in the best mode transistor. In other words, the size of transistors in Hspice determined in such a way that the lowest power consumption and minimal delay achieved (to determine the optimal W). To do this, we have V=0.13μ and W between values W_{max} and W_{min} the transistor model file is marked as 0.13μ and 100μ our Swipe. But here we have Swipe 6μ as for larger values for W, output from the ideal state is removed. The p-type transistor channel width should be 2 times the n-type (Fig.3).

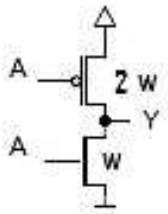
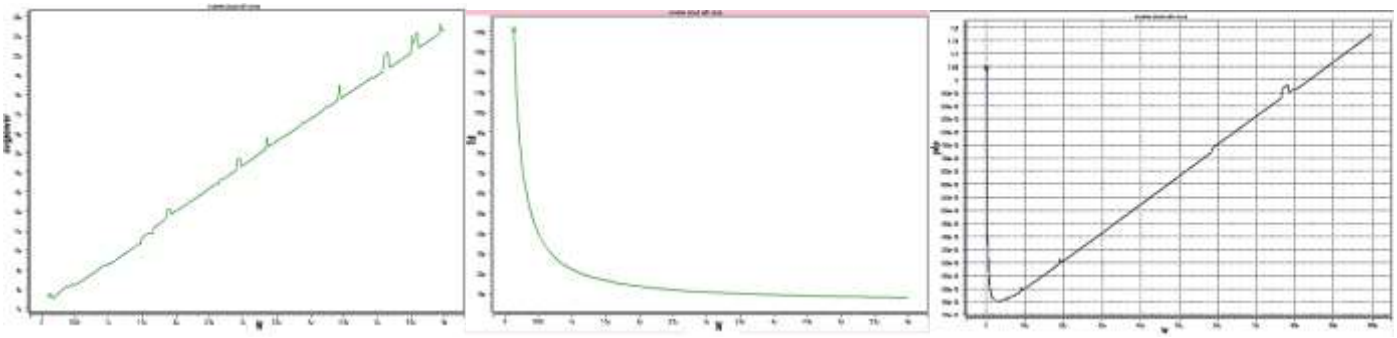


Figure 3: CMOS inverter circuit and transistor size network display pg and pd.

The charts can be, in terms of delay and PDP draw w. Graphs throughput, delay and PDP, respectively, in the form of fig.4 are shown. In each chart, the minimum point for comparison with the circuit CNTFET, obtains.



(a) (b) (c)

Figure 4: (a) Chart based on changes in average power consumption w, (b) Chart delay (td) in terms of changes w, (c) PDP graph according to w.

In the diagram Fig. 4(a), the lowest power consumption for w=0.13μ, $\text{avg power}_{\text{min}}$=7.64$\mu$ obtained. In graph w least delay, delay times td_{min}=7.8p, respectively (in the fall and rise delays as the delay circuit, whichever is greater). According to the chart PDP w, for w = 2.87μ, PDP_{min} = 149a, respectively.

For w = 2.87μ best PDP (lowest PDP) was obtained for the w, delay and average power by 10.7p, and 14 μ, respectively. The values obtained are summarized in Table 2 were brought.

Table 2: minimum amount of delay and average power inverter circuit PDP.

		w
Td_{min}	7.8p	6 μ
$\text{Avgpower}_{\text{min}}$	7.64 μ	0.13 μ
PDP_{min}	149a	2.87 μ

3.2. NOR Simulation with CMOS

In this circuit should be optimized for the inverter obtained from the w (w = 2.87 μ the inverter circuit was at least PDP), use. As in Figure 3has been found to be 4 times the width of the transistors is pu network.

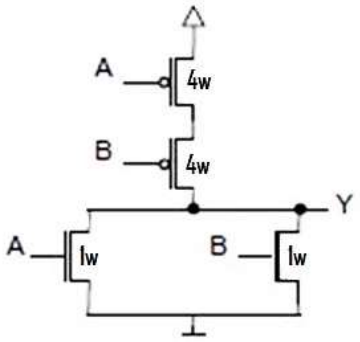


Figure 5: CMOS Circuit of NOR the size of the transistors and display networks pd and pu.

To get the THD should delay obtained on all tracks. Nor is it because the output circuit of 12 passes for 4 to switch the tracks so we need only calculate td related to the 4-pass. According to the truth table, we identified the 4 modes (Table 3) and delay for each individual obtains. Delays are to be calculated separately must zero in Hspice input B and input A applied to the circuit (Fig.6), and to obtain td_{rise1} and td_{fall1}. The zero input A and input B are applied to the circuit and to obtain td_{rise2} and td_{fall2}.

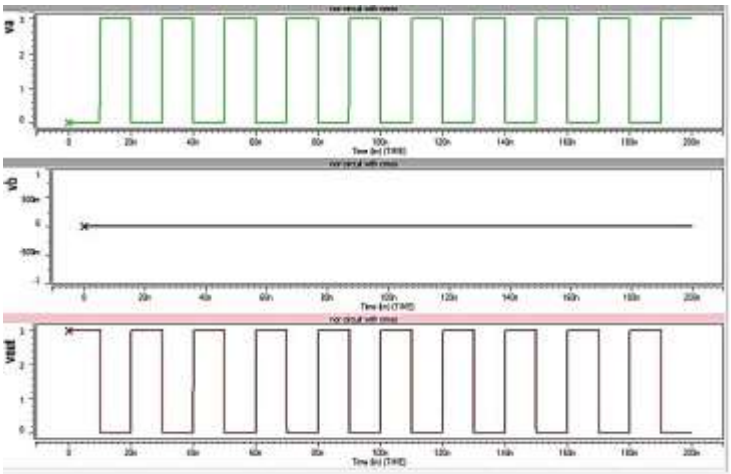


Figure 6: zero entry B and apply the AC input circuit for calculating td_{rise1} and td_{fall1}.

Table 3: NOR properly and passages that are changing the output mode.

A	B	Y=NOR(A,B)
0	0	1
0	1	0
1	0	0
1	1	0

(a)

A	B	Y	Name Delay	Delay
0	0→1	1→0	tdfall2	16.69p
0	1→0	0→1	tdrise2	13.13p
0→1	0	1→0	tdfall1	24.6p
1→0	0	0→1	tdrise1	16.98p

(b)

And the maximum amount of delay is considered as the main circuit delay. To calculate the PDP, the average power consumption should be multiplied by average rtd. Average power consumption avg power nor = 29.84u respectively.

$Td_{nor}=td_{max}=16.98p$
$avgpower_{nor}=29.84u$
$Avgtd_{nor}=(td_{fall1}+td_{fall2}+td_{rise1}+td_{rise2})/4=17.85p$
$Pdp_{nor}=Avgtd_{nor}*Avgpower_{nor}=532.644a$

3.3. NAND Simulation with CMOS

In this circuit, the optimal w obtained for the least PDP the inverter circuit, respectively (w = 2.87u), we use. Shape and width of transistors in the circuit shown below (Fig.7).

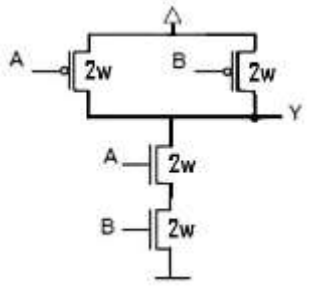


Figure 7: CMOS Circuit of NAND and display the size of transistors networks pd and pu.

In Table (4), 4 through which the output will change with the amount Delays.

Table 4: nand truth table and passages that are changing the output mode.

A	B	Y=NAND(A,B)
0	0	1
0	1	1
1	0	1
1	1	0

(a)

A	B	Y	Name Delay	Delay
1	0→1	1→0	tdfall2	13.03p
1	1→0	0→1	tdrise2	20.02p
0→1	1	1→0	tdfall1	10.47p
1→0	1	0→1	tdrise1	14.88p

(b)

The circuit delay, be average and PDP are given below.

$Td_{nand}=td_{max}=20.02p$
$Avgpower_{nand}=24.64u$
$Avgtd_{nand}=(td_{fall1}+td_{fall2}+td_{rise1}+td_{rise2})/4=14.6p$
$Pdp_{nand}=Avgtd_{nand}*Avgpower_{nand}=359.16a$

4. Simulation of CNTFET Circuits

4.1. Inverter simulation with CNTFET

In CNTFET transistors in order the changing some parameters, the value of power and delay change. Among these parameters, the gate length (Lgate) and the tube (the number of nanotube in a transistor) are.

To obtain the least possible delay, the first Swipe Lgate we (the tube to be desired) and the optimization of the chart Lgate PDP-Lgate (for minimum PDP) obtains. Then for this Lgate optimal value, we switch tube and the PDP-tube graph tube optimized value (for the lowest PDP) also obtains. So in this way the Lgate optimization and optimal tube is obtained.

The inverter circuit transistor size network CNTFET pu and pd are the same shape (Fig.8).

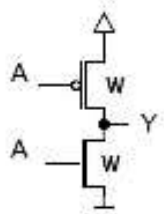
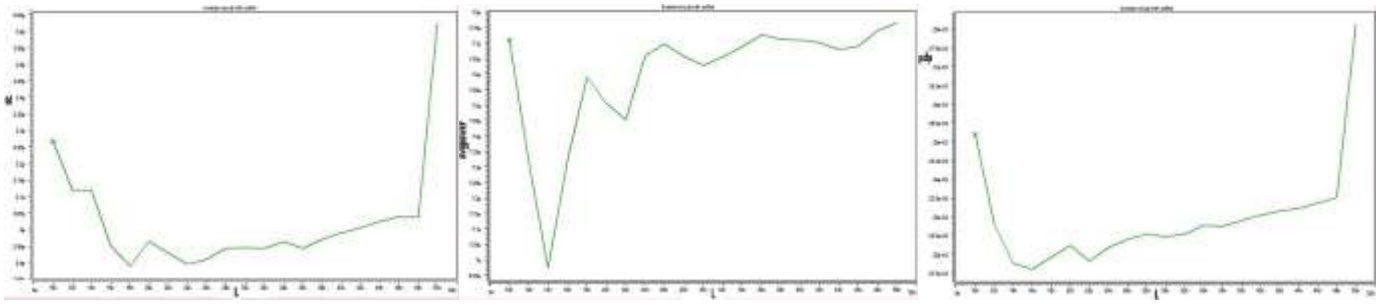


Figure 8: circuit transistor inverter with CNTFET and display size networks pd and pu.

In the form of fig.9, that in order to delay, and PDP are mean, for a desired amount of tube (tube=100), we Swipe gate length and minimum values obtained in the table 5 is given.



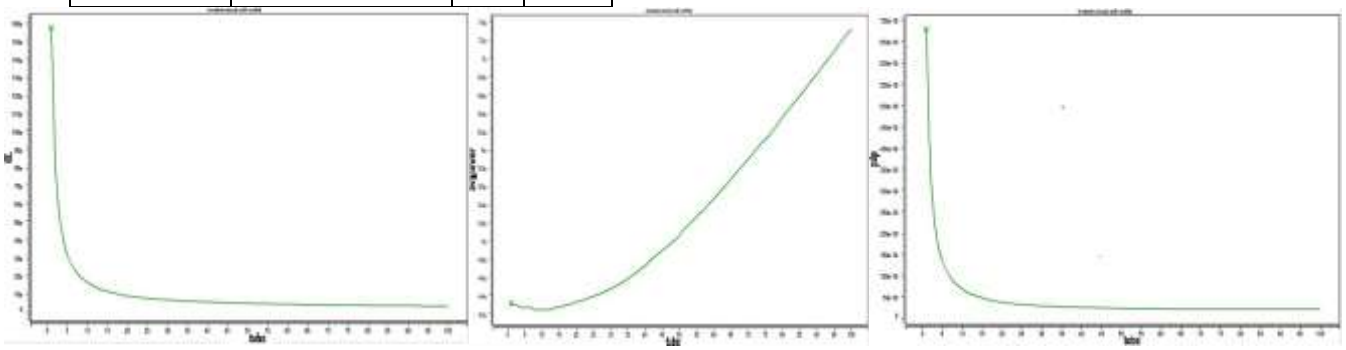
(a) (b) (c)

Figure 9: (a) Graph delay in changes L, (b) Average power consumption graph based on changes L, (c) PDP graph changes according to L.

Table 5: Values obtained minimum delay, power and PDP with Swipe L.

	Minimum value	**L**	**Tube**
Td	2.89p	18n	100
Avg power	6.97u	14n	100
Pdp	21.6a	16n	100

According to Table 4 above Gate optimum value for PDP, Lgate =16n, respectively. However, for the gate length (L=16n), the tube in the area where output is ideal, we Swipe. Stickers fig.10 that respectively delay, average power and PDP are, for Lgate=16n and Swipe obtained tube and minimum values in the table 6 is given.



(a) (b) (c)

Figure 9: (a) Delay Chart according to tube change, (b) Average power consumption graph according to tube change, (c) PDP graph according to tube change.

Pdp	21.3a	80	16n

According to the diagram fig. 10(a),(b) With the rise of tube delay circuit is low but the power consumption increases.

Table 6: Values obtained minimum delay, power and PDP with Swipe tube.

	Minimum value	**tube**	**L**
Td	2.95p	100	16n
Avg power	2.24u	9	16n

After reaching the lowest PDP shall optimal use Lgate =16n and tube = 80. The circuitry as CMOS circuitry supplement, not static power consumption. And only when switch power is consumed (Fig.11).

Figure 11: input voltage, output voltage and instantaneous power inverter circuit with CNTFET.

4.2. NOR Simulation with CNTFET

In this circuit Lgate and optimal tube obtained for the least PDP the inverter circuit was CNTFET (Lgate=16N and tube=80), we use. The width of the transistor in the circuit and is shown below.

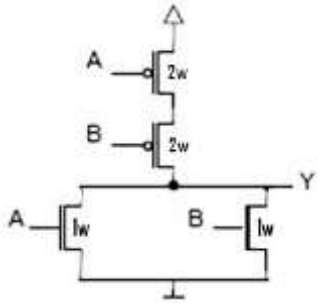


Figure 12: NOR Circuit with CNTFET and display the size of transistors networks pd and pu.

Table (6) 4 through which change can be output with the amount Delays.

Table 7: NOR truth table and passages that are changing the output mode.

A	B	Y=NOR(A,B)
0	0	1
0	1	0
1	0	0
1	1	0

(a)

A	B	Y	Name Delay	Delay
0	0→1	1→0	tfall2	2.66p
0	1→0	0→1	trise2	6.09p
0→1	0	1→0	tfall1	2.36p
1→0	0	0→1	trise1	4.88p

(b)

The circuit delay, be average and PDP are given below.

$Td_{nor}=td_{max}=6.09p$

$avgpower_{nor}=5.8u$

$Avgtd_{nor}=(td_{fall1}+td_{fall2}+td_{rise1}+td_{rise2})/4=3.99p$

$Pdp_{nor}=Avgtd_{nor}*Avgpower_{nor}=23.14a$

4.3. NAND Simulation with CNTFET

The circuit also obtained for the least PDP Lgate and optimal tube that was CNTFET inverter circuit (Lgate=16n and tube=80), we use. Shape and width of transistors in the circuit shown below (Fig.13).

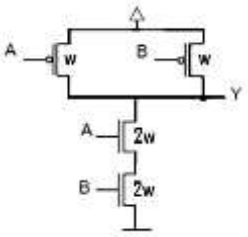


Figure 13: NAND Circuit with CNTFET and display the size of transistors networks pd and pu.

Table 8, 4 through which change can be output with the amount Delays.

Table 8: NAND truth table and passages that will change the output mode.

A	B	Y=NAND(A,B)
0	0	1
0	1	1
1	0	1
1	1	0

(a)

A	B	Y	Name Delay	Delay
1	0 → 1	1 → 0	tdfall2	4.7p
1	1 → 0	0 → 1	tdrise2	2.55p
0 → 1	1	1 → 0	tdfall	6.1p
1 → 0	1	0 → 1	tdrise1	2.69p

(b)

The circuit delay, be average and PDP are given below.

$Td_{nand}=td_{max}=6.1p$

$Avgpower_{nand}=5.87u$

$Avgtd_{nand}=(td_{fall1}+td_{fall2}+td_{rise1}+td_{rise2})/4=4.01p$

$Pdp_{nand}=Avgtd_{nand}*Avgpower_{nand}=23.54a\backslash$

5. Compare the results CMOS and CNTFET technology

As the table 9 is determined based on technology circuits CNTFET, compared to the technology CMOS (0.13 μ), in terms of delay, power consumption and PDP have between 70 to 90 percent improvement.

Table 9: Comparison of the results obtained from simulations

GATE	CMOS Technology			CNTFET Technology		
	Td	**Avg power**	**pdp**	**Td**	**Avg power**	**pdp**
INVERTER	7.8p	7.64u	149a	2.89p	4.24u	21.3a
NOR	24.6p	29.84u	532.6a	6.09p	5.8u	23.14a
NAND	20.02p	24.64u	359.16a	6.1p	5.87u	23.54a
AVG	17.47p	20.69u	346.92a	5.03p	5.3u	22.66a
Improvement vs. Cmos	-	-	-	71.2%	74.3%	93.46%

6. Designed inverter logic gate three (ternary) with transistors CNTFET

6.1. Summary of ternary logic

Tuesday is valued logic. 0, 1 and 2 respectively for false representation, defined and used correctly [10]. However, some of the undefined references 0, 1 and 2 indicate wrong is correct [11]. Each variable n {x 1, ..., X} of the ternary f (x) as a logical function mapping $\{0,1,2\}^n$ of {0,1,2} is defined in the x={x1,..., xn}. Ternary logic operations can be defined as low.

$$X_i, X_j \in \{0,1,2\} \Rightarrow \begin{cases} X_i + X_j = \max(X_i, X_j) \\ X_i . X_j = \min(X_i, X_j) \\ \overline{X}_i = 2 - X_i \end{cases}$$

(2)

Operators +,. And - to represent the practice of OR, and AND, NOT in their Ternary logic. The basic logic circuits ternary, inverter, Nor and Nand Gates are. Ternary logic symbols showed in the table 10.

Table 10: ternary logic symbols

LOGIC SYMBOLS

Voltage Level	Logic Value
0	0
1/2 V_{dd}	1
V_{dd}	2

Ternary logic gates based on the equations (2) are designed.

6.2. The definition of inversion in logic Ternary (three)

A typical inverter input of a single gate x, and 3 outputs (not defined y0, y1 and y2) are as follows.

$$y_0 = c_0(x) = \begin{cases} 2 \ if \ x = 0 \\ 0 \ if \ x \neq 0 \end{cases}$$

$$y_1 = c_1(x) = \overline{x} = 2 - x$$

(3)

$$y_2 = c_2(x) = \begin{cases} 2 \ if \ x \neq 2 \\ 0 \ if \ x = 2 \end{cases}$$

So, to implement an inverter ternary, 3 inverter is required. The 3 inverter, inverter negative ternary (NTI), the standard ternary inverter (STI) and inverter positive Ternary (PTI)

requirements. If y0, y1 and y2 output equations (3), the truth table of the table 11 is.

Table 11: Logic table Inverters STI, PTI and NTI

TRUTH TABLE OF STI, PTI, AND NTI

Input X	STI	PTI	NTI
0	2	2	2
1	1	2	0
2	0	0	0

6.3. NAND and NOR logic operation defined in ternary (triple)

This ternary logic gates are for multiple entries. Triple NAND and NOR logic input equations, functions as below.

$$Y_{NAND} = \overline{\min(X_1, X_2)} \quad (4)$$

$$Y_{NOR} = \overline{Max\{X_1, X_2\}} \quad (5)$$

Ternary logic gates NAND and NOR truth table (Table 12) are displayed.

Table 12: the right gate NOR and NAND.

TRUTH TABLE OF NAND AND NOR

Input X_1	Input X_2	Y_{NAND}	Y_{NOR}
0	0	2	2
1	0	2	1
2	0	2	0
0	1	2	1
1	1	1	1
2	1	1	0
0	2	2	0
1	2	1	0
2	2	0	0

6.4. NAND and NOR logic gates designed in three (ternary) with transistors CNTFET

Ternary logic NAND and NOR logic transistor CNTFET in equations 4 and 5 show. The circuits in Fig.14 have been brought.

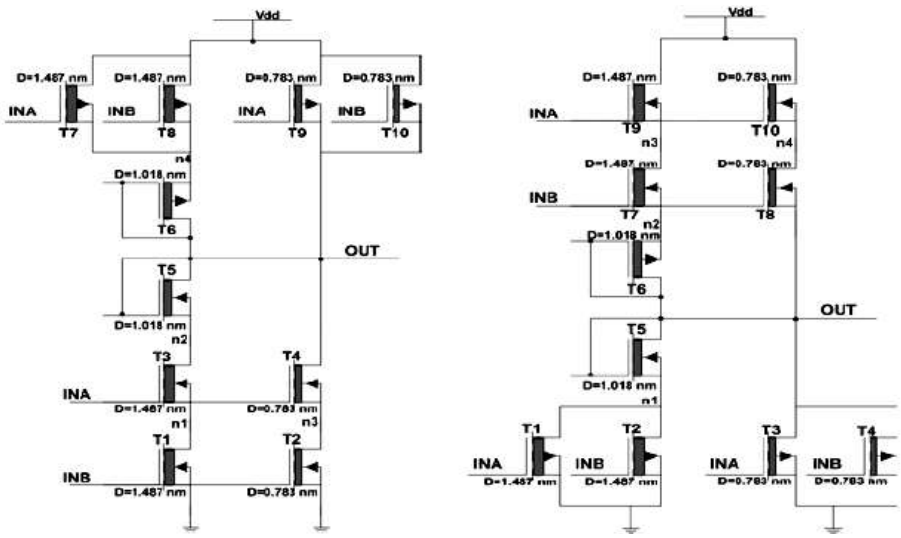


Figure 14: (a) NAND Gate, (b) NOR Gate.

Each transistor gate 10 CNTFET are three different chirality. They are similar to CMOS binary circuits except that the threshold voltages are different. The two gate like STI circuit in Fig. 14 , transistors with diameters 1.487nm, nm 0.783 and 1.018nm respectively threshold voltage v 0.289, v 0.559 and v 0.428 respectively

.

7. Conclusions

According to numerous studies that have been done CNTFET and optimization methods to solve their shortcomings to be challenged, despite many benefits that these devices are still a long way to MOSFET in industrial applications CNTFET there, As yet the growth of unwanted metal tubes during manufacture CNTs is an important challenge and a negative impact on delay, power and performance are CNT-based circuits. From this perspective, the theoretical and experimental results show clear vision to us. However, the scope for discussion, exchange of ideas and research takes more and more widespread.

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