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Power reduction in digital VLSI circuits

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ABSTRACT

The increased use of Portable electronics devices such as cellular phones, notebook and computers has made power dissipation an important design metric in modern microelectronics. Portable devices that operate using a battery have limited energy supplies and thus have lifetime that are constrained by their power consumption. Even ICs in systems that are plugged into a continuous power supply are becoming power constrained due to the difficulty of dissipating heat that results from consuming power on a chip with many tightly packed transistor. Our objective is to reduce power dissipation in digital CMOS VLSI circuits.later; we will compare all the optimal methods which can reduce maximum power dissipation among all and with fewer limitations. We have used Galaxy Custom Designer a tool of Synopsys and SPICE coding to find out delay, power, energy and leakage charge with the various design styles like CMOS, Pass transistor, DCVS (Differential cascade voltage switch logic circuit), Dynamic, DCVS-PG. We had computed the delay, power, energy and power leakage and compared amongst these design styles to conclude which design style would work for the specific requirement.

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VLSI, power reduction, design methodology for VLSI circuits, CMOS Implementation, power and delay of CMOS circuit

1.Introduction

The increased use of portable electronic devices (such as cellular phones and notebook computers) has made power dissipation an important design metric in modern microelectronics. Portable devices that operate using a battery have a limited energy supply and thus have lifetimes that are constrained by their power consumption. Technology continues to scale down; leakage power has become an ever-increasing important part of the total power consumption of a chip. Techniques for low-power operation are shown which use the lowest possible supply voltage coupled with architectural, logic style, circuit, and technology optimizations.

1.1 Why to reduce the power

Until now, the power consumption has not been of great concern because of the availability of large packages and other cooling techniques having the capability of dissipating the generated heat. However, continuously increasing density as well as the size of the chips and systems might cause difficulty in providing adequate cooling and hence, might either add significant cost to the system or provide a limit on the amount of the functionality that can be provided. Another factor that fuels the need for low-power chips is the increased market demand for portable consumer electronics powered by batteries. For these high performance portable digital systems, running on batteries such as-laptops, cellular phones and personal digital assistants (PDAs), low-power consumption is a prime concern because it directly affects the performance by having effects on battery longevity. Hence, low-power VLSI design has assumed great importance as an active and rapidly developing field. Due to their extreme low-power consumption, subthrehsold design approaches are appealing for a widening class of applications which demand low-power consumption and can tolerate larger circuit delays.

1.2 power dissipation in vlsi circuits

In digital VLSI circuit, there is power dissipation due to leakage current, switching transition current and charging and discharging of load capacitances. There are basically two types of power dissipation in digital VLSI:

1) Static power dissipation: is due to leakage current
2) Dynamic power dissipation: is due to:
a) Switching transient current
b) Charging and discharging of load capacitances.

2.Theory

Table1: number of transistors required for design styles for **n** number of inputs in various design styels –

Design Style	Number of Transistor Requires
CMOS	2N
Pseudo or Ratioed	N+1
DCVS	2N+2
Dynamic	N+2

The characteristics and behaviour of the design styles have been shown below

CMOS –

1. Static Power Dissipation= 0
2. Connected to low resistance path

3. Full Swing 0 to Vdd.
4. Higher Noise Margin

Pseudo –

1. Less number of Transistors
2. Area would reduce
3. Less Complexity
4. Unwanted delay would reduce
5. Power will be more

DCVS –

1. Gives Circuit and its complemented in output
2. More number of transistors required
3. More Area would be required.

Dynamic-

1. Depends on clock
2. Pre charge and Evaluation conditions

3.Observations

The average power has been observed from 1ns to 20ns and the HSPICE command used is as follows –

.measure tran avgpwr AVG power from = 1ns to = 20ns

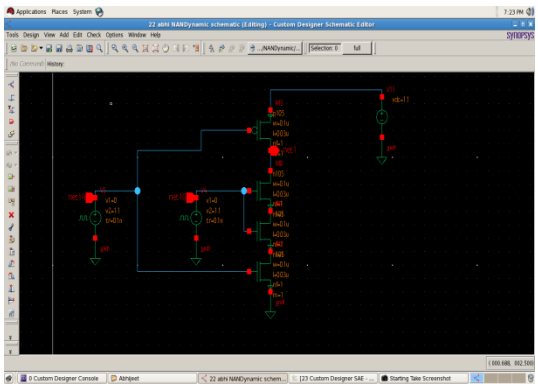


Fig.1: Dynamic Circuit of NAND Gate

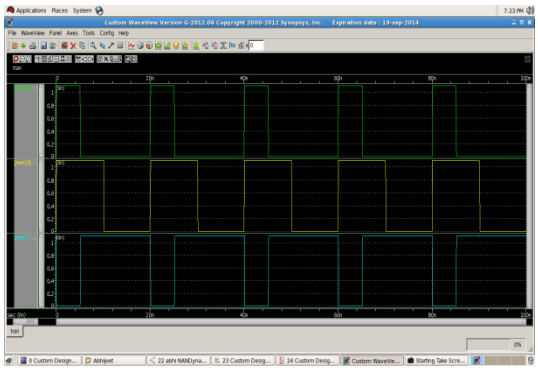


Fig.2: the output waveform verification

These all observations have been taken by with the following values of VPULSE (Input signal) for A, B, Abar and Bbar.

Table 2: fix input parameter during work

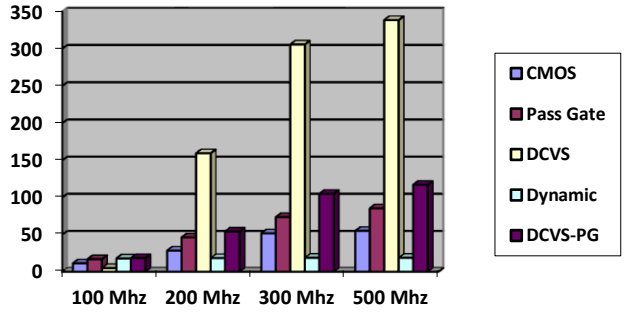
	A	B	Abar	Bbar
V1	0	0	1.1v	1.1v
V2	1.1v	1.1v	0	0
T_r	0.1ns	0.1ns	0.1ns	0.1ns
T_f	0.1ns	0.1ns	0.1ns	0.1ns
Tdelay	5ns	10ns	5ns	10ns
Duration	10ns	20ns	10ns	20ns

Here,
T_r = rise time, T_f = fall time

3.1 Average power of 2-input NAND Gate for 1ns to 20ns with different circuit implementations

TABLE 3: POWER OF DESIGN STYLES WITH FREQUNCY (IN nw)

	100mhz	200mhz	300mhz	500mhz
CMOS	11.3646	28.5002	51.7824	55.0666
Pass gate	16.9793	46.3026	73.5745	85.4828
DCVS	4.98520	159.637	305.652	338.486
Dynamic	18.0043	18.4705	18.8701	18.8978
DCVS-PG	18.4822	54.2053	104.902	117.123



Graph1: Average power presentation with frequency variations in different design styles.

It has been observed that The Ratioed and Pseudo have power dissipation more than other design styles, while CMOS and Dynamic implementations shows low Power Dissipation. At very low frequency (100 MHz) DCVS is giving lowest Power consumption but at higher frequencies (f>100 MHz) it's giving maximum Power dissipation. In case of Dynamic its behaviour is nearly constant for all frequencies and showing very less Power consumption as compared to others if we see at bundle of frequency. For CMOS, PASS, DCVS-PG the power is depending on the frequency, at the higher frequencies the power dissipation is also increasing.

3.2 DELAY - we can find the delay by the following formula,

$$\tau = \tau_{PHL} + \tau_{PLH}/2$$

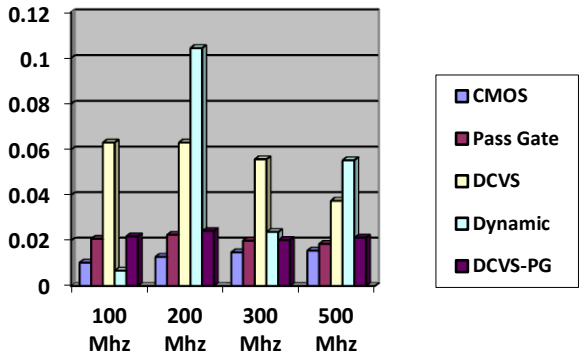
τ_{PHL} =TIME taken by output to change from high to low state

τ_{PLH} =TIME taken by output to change from low to High state

With the same input values we find the delay with various techniques and results are as follows –

Table 4: Delay of design styles with frequency (in ns)

	100mhz	200mhz	300mhz	500mhz
CMOS	0.01030	0.01293	0.014835	0.01562
Pass gate	0.02073	0.02252	0.019940	0.01856
DCVS	0.06946	0.06309	0.055774	0.03754
Dynamic	0.00680	0.01044	0.023795	0.05534
DCVS-PG	0.02186	0.02422	0.020250	0.02129



Graph2: Delay of different design styles with frequency

CMOS is showing constant and very low delay for all the frequencies where as in Pass transistor, the delay is inversely proportional to frequency, at increasing frequencies its delay reduces. Dynamic is showing less delay or nearly equal to CMOS for low frequency .DCVS PG also shows constant and low delay with respect to frequencies.

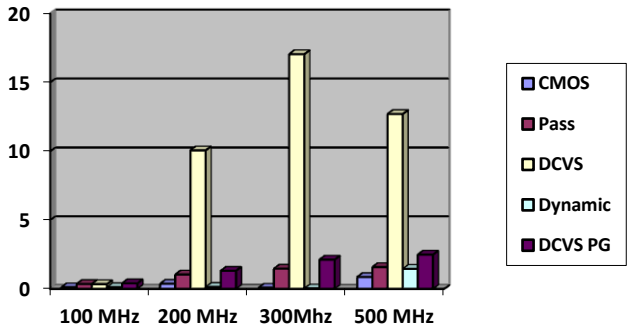
3.3 Energy

Energy can be determined by the product of Power and Delay.

Energy = Power * Delay

Table5: Energy of various design style with frequency

Frequency	100 MHz	200 MHz	300Mhz	500 MHz
CMOS	0.117055	0.368507	0.085781	0.860140
Pass	0.351980	1.042966	1.467075	1.586560
DCVS	0.346274	10.07234	17.04743	12.70761
Dynamic	0.122429	0.140632	0.033003	1.458043
DCVS PG	0.404020	1.313123	2.124269	2.494142



Graph3: Energy of different design styles with frequency

Hence, with these observations we can find that CMOS and Dynamic implementation provide better result in terms of energy while the DCVS is consuming higher energy than other implementation techniques.

We have considered an important parameter to fulfil our objective and hence we have considered leakage power too.

3.4 Leakage Power

Leakage Power = Energy / T = (Leakage charge * voltage) / T

The voltage is constant for all so we can simplify by considering constant time duration, we can find leakage charge so that we can compare it for leakage power.

It has been taken for 0 to 40ns duration –

Table 6: leakage power of various design styles with respect to frequency

Design style	Leakage charge
CMOS	0.005922 fC
Dynamic	0.014396 fC
DCVS	1.104330 fC
DCVS-PG	0.548363 fC
Pass	0.574533 fC

With this observation it can be analysed that CMOS and Dynamic have less leakage power comparing to others and DCVS technology gives us larger leakage power. So from the above table we can see that the less leakage power is shown by CMOS and Dynamic

So now we verify how it really better than other design techniques.

Comparison between 2 best Design Styles -

We have seen that if we take Power Consumption and Delay and energy and Leakage power as our parameters and we compare all the design styles as we did earlier than we could come up with the 2 best design styles, they are –

CMOS and Dynamic

So we will now cross-check for Half – adder circuit and will determine whose design style is better at what conditions.

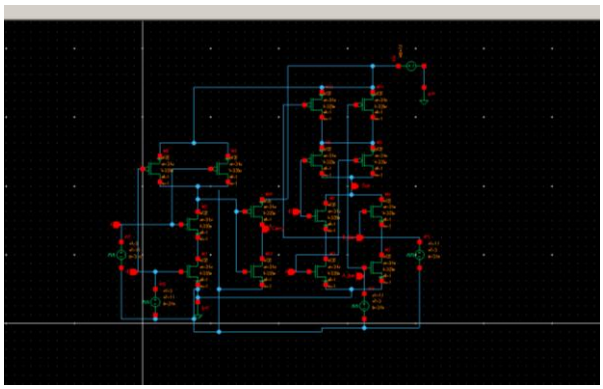


Fig 3: Schematics of half adder circuit in cmos circuit designing.

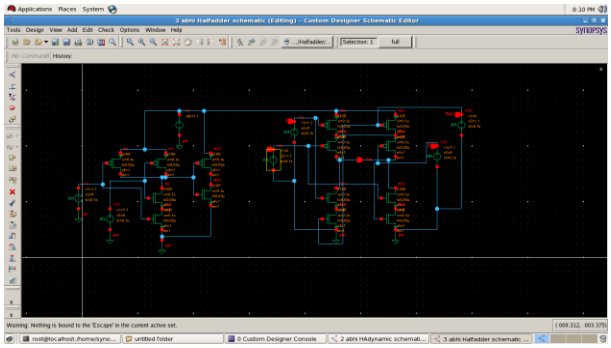


Fig. 4: Half Adder Circuit in Dynamic Style

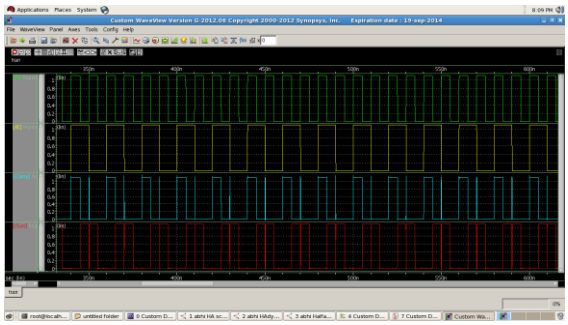


Fig. 5: Output Verification of Half Adder Circuit

Parameter comparisons –
Average Power of CMOS = 82.9580 n
Average Power of Dynamic = 62.8058n
Observations has been taken from 0ns to 40ns

Delay –
Delay of Sum of CMOS = 0.019645 n
Delay of Sum of Dynamic = 0.013825 n
Delay of Carry of CMOS = 0.025775n
Delay of Carry of Dynamic = 0.024255n

4.Conclusion

The Average Power dissipation CMOS is higher than Dynamic so if power is our concern, then it has been observed that the circuit can be designed in Dynamic Design styles for better performance.
Delay of Dynamic is less than CMOS Design style, so if Power consumption and Delay is the concern parameter, then it has been suggested to use DYNAMIC Design Style for better performance.

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